32.7 A Combined Dynamic and Static Frequency Divider for a 40GHz PLL in 80nm CMOS

George von Büren[1], Christian Kromer[1], Frank Ellinger[1], Alex Huber[2], Martin Schmatz[3], Heinz Jäckel[1]

[1]ETH, Zürich, Switzerland
[2]ZMA, Windisch, Switzerland
[3]IBM, Rüschlikon, Switzerland

Future high-density chip-to-chip links require data rates of up to 40Gb/s per channel to meet the Tb/s aggregate bandwidth demand. A transmitter and receiver incorporate D-flip-flops (DFF), consisting of two latches (TFF) to retime the data, ideally at full speed. The clock driving the DFFs is generated by a PLL, which therefore requires a full-rate frequency divider in the CMU. The prescaler typically is the speed-limiting block. In addition, because of the limited system power budget, all circuits need to be optimized for low power consumption. Consequently, the design of low-power and high-speed frequency dividers is a challenging task.

The implemented circuit shown in Fig. 32.7.1 consists of a dynamic and a static frequency divider followed by a 50Ω buffer for test and measurement equipment. Conventional static frequency dividers (SFD) use a DFF, which allows broadband operation from dc to a maximum division frequency. As long as the slew rate of the input signal is high enough, the maximum division frequency of a static frequency divider is approximately $1/(2t_{pd})$, where t_{pd} denotes the latch propagation delay. Higher operating frequencies can be achieved by dynamic frequency dividers (DFD), based on Miller's work in 1939 on regenerative modulation, because the loop contains only one t_{pd} instead of two. Therefore, a DFD is chosen for the first divider stage. The limited operating range does not pose a problem for most applications where the divider only operates in a narrow frequency range. Fig. 32.7.1 shows the block diagram for a regenerative frequency divider consisting of a mixer, a filter and an amplifier. Assuming an input signal f_{in} and a feedback signal f_{out}, the mixer output signal has the frequency components $f_{in} \pm f_{out}$. Only the component $f_{in} - f_{out}$ can pass the filter and, consequently, stable operation exists if $f_{out} = f_{in} - f_{out} = f_{in}/2$. The operating bandwidth is limited by the band-pass frequency response of the open loop. The maximum operating frequency limit is reached when the open-loop gain is 1 at $f_{in}/2$. The lower limit for frequency division is obtained when the filter no longer suppresses the frequency component $3f_{in}/2$ or when the open-loop gain falls below 1 at $f_{in}/2$.

Most Miller dividers incorporate a double-balanced Gilbert cell mixer realized with RF-port feedback [1] or LO-port feedback [2]. In contrast to a SFD where the load impedance generates a logic swing, the role of the load of the DFD is to convert the desired current component mixed by the Gilbert cell to a voltage. Bipolar implementations introduce source followers in the feedback loop to provide level shifting, sufficient broadband gain around the loop at $f_{in}/2$ and suppression of higher-order odd-harmonic components at $3f_{in}/2$, $5f_{in}/2$… due to the inherent low-pass characteristic of the mixer. Operating frequencies over one octave can be achieved [1]. The design challenge of a CMOS broadband regenerative divider is the design of a feedback network featuring a low output impedance, a voltage gain > 1 and minimum delay. A DFD operating from 17 to 27GHz in 0.13µm CMOS was recently reported [2]. The feedback consists of a differential amplifier stage responsible for filtering out $3f_{in}/2$ followed by an inductively-peaked differential stage to amplify $f_{in}/2$. Employing a BPF in the Miller divider increases the operating frequency. In contrast to the 38 to 41GHz DFD presented in [3] with a power consumption of 42mW, the DFD shown here dissipates only 2.2mW, a factor of 19 less.

Figure 32.7.2 shows the schematic of the DFD. The input is fed to the LO-port ($M1$ to $M4$) and the mixer output is connected to the RF-port via the feedback network consisting of a combination of a common-source stage and a source follower [4]. $M7$ and $M8$ are low-threshold-voltage (LVT) FETs to diminish their overdrive voltages. $M9$ and $M10$ are high-threshold-voltage (HVT) FETs to extend the saturation region of the transistors for large-signal operation. Transistors $M7$ to $M10$ perform level shifting, isolate the high-impedance node at the mixer output and drive the RF-port and the following frequency divider. The advantage of the proposed feedback topology is that the voltage gain can be >1, whereas a source-follower always has a gain <1. Furthermore, the frequency-dependent phase shift is smaller at high frequencies because of the lowered output impedance of the source follower. Because of the large loop gain, the Q of the band-pass load can be decreased to broaden the operating range. The load consists of a 140Ω resistor and a spiral inductor having a series inductance and resistance of 3nH and 88Ω, respectively. The inductor occupies four metal layers with an area of 15µm×15µm and can handle a maximum dc current of 0.8mA. The simulated open-loop band-pass frequency response of the DFD showing the operating region at $f_{in}/2$ is depicted in Fig. 32.7.3.

The TFFs of the SFD (Fig. 32.7.4) are optimized for low power consumption and minimum input amplitude at 20GHz. To decrease the rise and fall times of the SFD, peaking inductors with series inductance and resistance of 2nH and 75Ω, respectively, have been added in series with the 1kΩ load resistance.

All measurements of the divide-by-four and SFD circuits were performed on the wafer. In contrast to the DFD, the SFD self-oscillates if no input power is applied. The measured self-oscillation frequency of the SFD is 11GHz. The measured and simulated minimum single-ended input amplitude curves for correct division for the SFD and the divide-by-four circuits are shown in Fig. 32.7.5. The operating range of the divide-by-four circuit is from 31 to 41GHz. The measured output spectrum of the divide-by-four circuit with a 40GHz input amplitude of $0.4V_{pp}$ is shown in Fig. 32.7.6 and exhibits a phase noise of -105dBc/Hz at 500kHz offset. The current consumption of the DFD is 2mA and the Gilbert cell and the feedback network consume 1mA each. The SFD consumes 1mA and the output buffer 26mA. The circuits operate with a 1.1V supply.

Figure 32.7.7 shows a micrograph of the divide-by-four frequency divider including the output buffer fabricated in a standard 8M CMOS process with a nominal transistor gate length of 80nm. The DFD and SFD occupy 20µm×60µm and 20µm×30µm, respectively.

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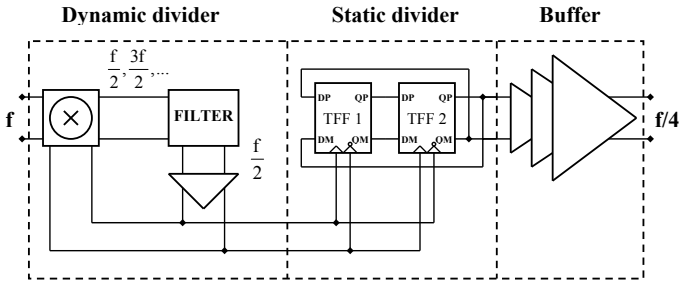

Figure 32.7.1 The block diagram of the regenerative frequency divider.

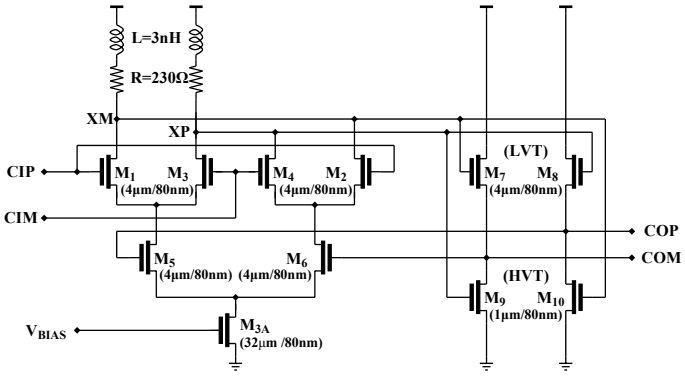

Figure 32.7.2 Schematic of the DFD.

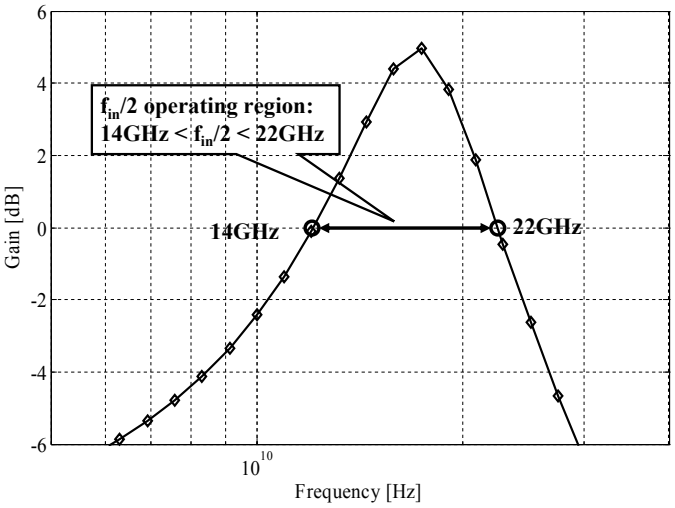

Figure 32.7.3 Simulated open-loop frequency response of the DFD.

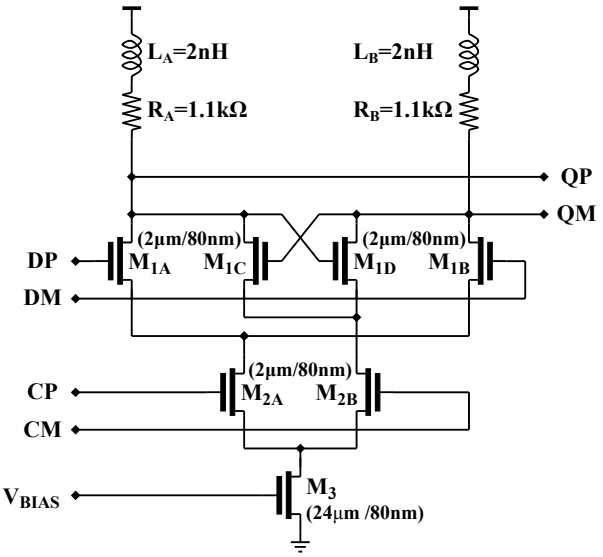

Figure 32.7.4 Static frequency divider schematic.

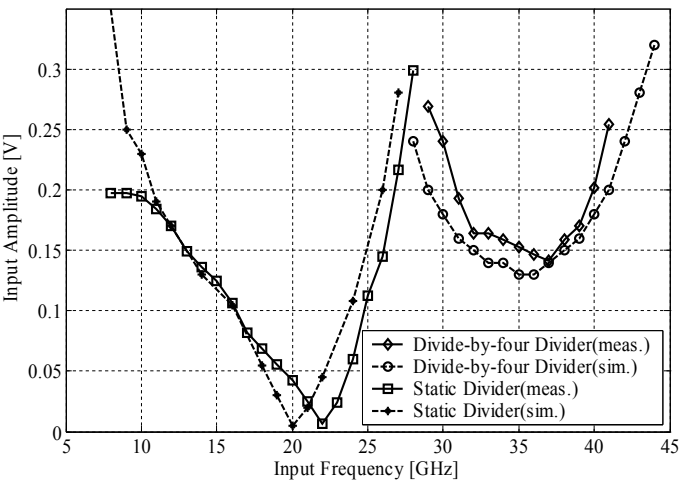

Figure 32.7.5 Measured and simulated minimum single-ended input amplitude curves for correct division

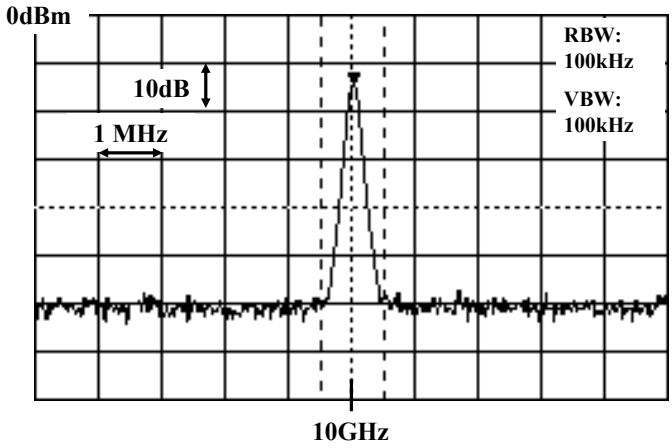

Figure 32.7.6 Measured output spectrum of the divide-by-four circuit.

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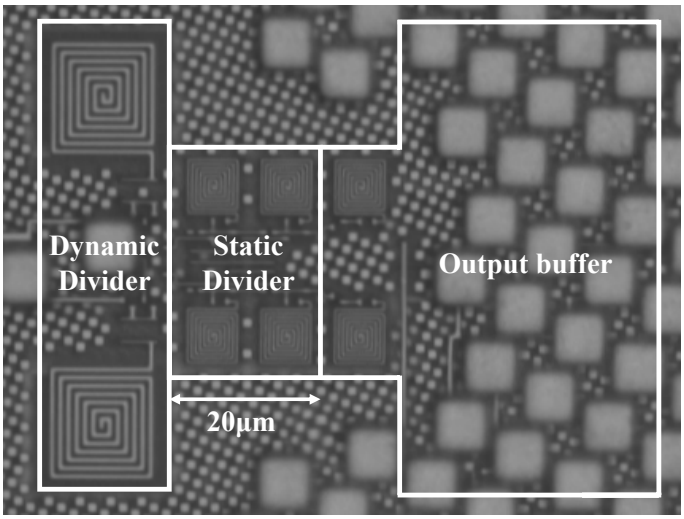

Figure 32.7.7 Chip micrograph.

